WHAT IS CLAIMED IS

1. A probe card for testing a semiconductor chip, comprising:

a plurality of probes;

a build-up interconnection layer having a multilayer interconnection structure therein, said build-up interconnection layer carrying said plurality of probes on a top surface thereof in electrical connection with said multilayer interconnection structure; and

a capacitor embedded in a resin insulation layer constituting said build-up interconnection layer in electrical connection with one of said probes via said multilayer interconnection structure,

said multilayer interconnection structure including an inner via-contact in the vicinity of said probe.

2. A probe card as claimed in claim 1, wherein said capacitor has a thickness generally equal to or less than a thickness of said resin insulation layer.

3. A probe card as claimed in claim 1, wherein said capacitor is formed on a silicon substrate having a polished bottom surface and includes a structure sandwiching a dielectric film by

upper and lower electrode films, said structure being formed on a top surface of said silicon substrate.

4. A probe card as claimed in claim 1, wherein said capacitor is formed in said build-up interconnection layer, right underneath one of said probes.

5. A probe card as claimed in claim 1, wherein said probe card includes therein a plurality of said capacitors, said capacitors being connected to respective power lines of different supply voltages.

6. A probe card as claimed in claim 1, wherein said capacitor includes a dielectric film of a complex oxide containing at least one metal element selected from the group consisting of Sr, Ba, Pb, Zr, Bi, Ta, Ti, Mg and Nb.

7. A probe card as claimed in claim 1, wherein said capacitor includes an upper and lower electrodes sandwiching a dielectric film, said first and second electrodes containing at least one metal element or a metal oxide selected from the group consisting of Pt, Au, Cu, Pb, Ru, a Ru oxide, Ir, an

Ir oxide, and Cr.

8. A probe card as claimed in claim 1, wherein said capacitor has a thickness of 30 μm or less, said thickness including a thickness of a support substrate on which said capacitor is formed and a height of a terminal electrode.

9. A probe card as claimed in claim 1, wherein said capacitor is a thin-film capacitor formed on a support substrate and has a laminated structure formed on said support substrate, said laminated structure including a dielectric film sandwiched by upper and lower electrode films.

10. A testing method of a semiconductor device by using a probe card,

said probe card comprising: a plurality of probes; a build-up interconnection layer having a multilayer interconnection structure therein, said build-up interconnection layer carrying said plurality of probes on a top surface thereof in electrical connection with said multilayer interconnection structure; and a capacitor embedded in a resin insulation layer constituting said build-up interconnection layer in electrical connection with one of said probes via said multilayer interconnection structure, said multilayer interconnection structure

including an inner via-contact in the vicinity of said probe,

said method comprising the steps of:

causing said probe card to make a contact with a semiconductor chip to be tested such that said semiconductor chip is in electrical connection with said probe card; and

testing electric properties of said semiconductor chip,

said method further comprising the step, before contacting said probe card to said semiconductor chip, of setting an impedance between said probe and said capacitor to be substantially equal to an impedance of a semiconductor package including therein said semiconductor chip and a capacitor, for a part between said semiconductor chip and said capacitor.

11. A testing method as claimed in claim 10, wherein said test is conducted in the state said semiconductor chip forms a semiconductor wafer.

12. A probe card for testing a semiconductor chip, comprising:

a first interconnection substrate;

a second interconnection substrate mounted on said first interconnection board in such a manner that a gap is formed between said first interconnection substrate and said second interconnection substrate;

a plurality of probes provided on said

second interconnection substrate at a surface away form said first interconnection substrate; and

a decoupling capacitor provided on said second interconnection substrate at a surface facing said first interconnection substrate.

13. A probe card as claimed in claim 12, wherein said first interconnection substrate includes therein an interconnection structure including an inner via-contact, said second interconnection substrate having a thickness of 1mm or less.

14. A probe card as claimed in claim 12, wherein said decoupling capacitor is a thin-film capacitor formed on a support substrate and has a laminated structure formed on said support substrate, said laminated structure including a dielectric film sandwiched by upper and lower electrode films.

15. A probe card for testing a semiconductor chip, comprising:

a first interconnection substrate;

a second interconnection substrate mounted on said first interconnection substrate such that there is formed a gap between said first interconnection substrate and said second interconnection substrate; and

a plurality of probes provided on said

second interconnection substrate at a surface away from said first interconnection substrate,

a difference of thermal expansion coefficient between said first interconnection substrate and said second interconnection substrate is 2ppm/℃ or less.

16. A probe card as claimed in claim 15, wherein said second interconnection substrate has a thermal expansion coefficient of 4 ± 2ppm/℃.

17. A probe card as claimed in claim 15, wherein said second interconnection substrate carries, on a surface thereof facing said first interconnection substrate, a decoupling capacitor.

18. A probe card as claimed in claim 15, wherein said second interconnection substrate includes an interconnection layer formed on a surface of any of a resin-infiltrated carbon fiber board and an invar board.

19. A probe card as claimed in claim 15, wherein said first interconnection substrate and said second interconnection substrate are connected by a

pin grid array.

20. A probe card as claimed in claim 15, wherein said first interconnection substrate and said second interconnection substrate are connected detachably.

21. A probe card as claimed in claim 15, wherein said first interconnection substrate carries, on a surface away from said second interconnection substrate, a pin electronic module in a detachable manner.

22. A testing method of a semiconductor chip by using a probe card,

said probe card comprising: a first interconnection board; a second interconnection board mounted on said first interconnection board in such a manner that a gap is formed between said first interconnection board and said second interconnection board; a plurality of probes provided on said second interconnection board at a surface away form said first interconnection board; and a decoupling capacitor provided on said second interconnection board at a surface facing said first interconnection board,

said method comprising the step, before contacting said probe card to said semiconductor chip,

of setting an impedance between said probe and said capacitor to be substantially equal to an impedance of a semiconductor package including therein said semiconductor chip and a capacitor, for a part between said semiconductor chip and said capacitor.

23. A testing method as claimed in claim 22, wherein said probe card has impedance between said probe and said decoupling capacitor set to fall within a range of -50% and +100% of the impedance of the semiconductor chip to be tested and a decoupling capacitor connected to said semiconductor chip in a semiconductor device product.

24. A capacitor, comprising:

a dielectric film;

a first electrode film formed on a first principal surface of said dielectric film;

a second electrode film formed on a second principal surface of said dielectric film;

a first interconnection part extending from said first electrode film to a first side of a laminated structure formed of said dielectric film and said first and second electrode films; and

a second interconnection part extending from said second electrode film to said first side,

a resin layer being formed on a second side of said laminated structure.

25. A capacitor as claimed in claim 24, wherein said capacitor carries another resin layer at

said first side of said laminated structure, said first interconnection part and said second interconnection part being exposed at a surface of said another resin layer.

26. A capacitor as claimed in claim 24, wherein said capacitor has a total thickness, defined as a thickness from a bottom surface of said resin layer to a top surface of said first and second interconnection parts, of 10 μm or less.

27. A capacitor as claimed in claim 24, wherein said first and second interconnection parts form respective contactors such that the contactors are aligned on a substantially flush plane.

28. A capacitor as claimed in claim 24, wherein said resin layer is selected from the group consisting of a polyimide resin, an epoxy resin, a bismaleimide triazine resin, a polytetrafluoroethylene resin, a benzocylcobutene resin, an acryl resin, and diallyl phtalate resin.

29. A capacitor as claimed in claim 24, wherein said resin layer has a surface roughness of

5nm or less.

30. A semiconductor device, comprising:

a capacitor; and

a semiconductor chip on which said capacitor is mounted;

said capacitor comprising: a dielectric film; a first electrode film formed on a first principal surface of said dielectric film; a second electrode film formed on a second principal surface of said dielectric film; a first interconnection part extending from said first electrode film to a first side of a laminated structure formed of said dielectric film and said first and second electrode films; and a second interconnection part extending from said second electrode film to said first side, a resin layer being formed on a second side of said laminated structure.

31. A method of manufacturing a capacitor, comprising the steps of:

forming a first insulation film of a resin on a substrate;

forming a first electrode film on said first insulation film;

forming a dielectric film on said first electrode film;

forming a second electrode film on said dielectric film; and

removing said substrate by an etching

process such that said first insulation film is exposed.